IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Previously presented) A method for fabricating a chip-scale package, comprising:

positioning a sacrificial substrate adjacent to a back side of a device substrate with a plurality of conductive elements on an active surface of the sacrificial substrate being aligned along at least one street between adjacent semiconductor devices on an active surface of the device substrate;

securing the active surface of the sacrificial substrate to the back side of the device substrate with a quantity of dielectric material electrically isolating each conductive element of the plurality of conductive elements from the back side of the device substrate;

severing the device substrate to physically separate the adjacent semiconductor devices from one another and to form peripheral edges of each semiconductor device of the adjacent semiconductor devices, relative positions of the adjacent semiconductor devices being maintained by the sacrificial substrate;

forming a dielectric coating on at least portions of at least some of the peripheral edges;

exposing at least portions of at least some conductive elements of the plurality of conductive elements, each exposed conductive element comprising a lower section of a contact pad of the chip-scale package; and

forming a peripheral section of the contact pad in communication with a corresponding lower section and on a peripheral edge of a semiconductor device.

2. (Previously presented) The method of claim 1, further comprising:

forming a redistribution layer on the active surface of the device substrate and in electrical isolation from circuitry of an underlying semiconductor device.

3. (Previously presented) The method of claim 2, wherein forming the dielectric coating includes forming a dielectric coating over at least portions of the active surface of the device substrate.

4. (Previously presented) The method of claim 3, wherein forming the dielectric coating over at least portions of the active surface of the device substrate electrically isolates at least one conductive trace of the redistribution layer from circuitry of an underlying semiconductor device.

5. (Previously presented) The method of claim 2, wherein forming the redistribution layer is effected before severing.

6. (Previously presented) The method of claim 5, wherein severing includes severing at least one conductive trace of the redistribution layer.

7. (Previously presented) The method of claim 2, further comprising:
forming an upper section of the contact pad in communication with both the peripheral section and a conductive trace of the redistribution layer and over at least one semiconductor device of the adjacent semiconductor devices.

8. (Previously presented) The method of claim 1, further comprising:
forming an upper section of the contact pad in communication with the peripheral section and over at least one semiconductor device of the adjacent semiconductor devices.

9. (Previously presented) The method of claim 1, further comprising:
removing at least a portion of the sacrificial substrate to facilitate separation of the adjacent semiconductor devices from one another.

10. (Previously presented) The method of claim 9, wherein removing comprises substantially removing the sacrificial substrate.

11. (Previously presented) The method of claim 10, wherein substantially removing comprises back grinding the sacrificial substrate.

12. (Previously presented) The method of claim 1, wherein securing comprises use of a dielectric adhesive material.

13. (Previously presented) The method of claim 1, wherein severing is effected into the dielectric material.

14. (Previously presented) The method of claim 1, wherein forming the dielectric coating comprises introducing dielectric material into at least one recess formed by severing.

15. (Previously presented) The method of claim 14, wherein introducing comprises forming a layer comprising the dielectric material over at least a portion of the active surface of the device substrate.

16. (Previously presented) The method of claim 14, wherein introducing comprises introducing a dielectric polymer into the at least one recess.

17. (Previously presented) The method of claim 14, wherein introducing comprises substantially filling the at least one recess with the dielectric material.

18. (Previously presented) The method of claim 17, further comprising severing the dielectric material to re-separate the adjacent semiconductor devices from one another.

19. (Previously presented) The method of claim 18, wherein exposing is effected substantially concurrently with severing the dielectric material.

20. (Previously presented) The method of claim 1, wherein positioning comprises positioning the device substrate such that the at least one street is aligned over at least some conductive elements of the plurality of conductive elements.

21. (Previously presented) The method of claim 20, wherein exposing comprises severing the at least some conductive elements.

22. (Previously presented) The method of claim 1, wherein positioning comprises positioning the device substrate such that the at least one street is aligned between an adjacent pair of conductive elements of the plurality of conductive elements.

23. (Previously presented) The method of claim 1, further comprising:
forming a temporary protective layer over at least a portion of each of the adjacent semiconductor devices prior to forming the dielectric coating.

24. (Previously presented) The method of claim 23, wherein forming the temporary protective layer is effected prior to severing.

25. (Previously presented) The method of claim 23, wherein forming the temporary protective layer comprises forming the temporary protective layer over an optical element comprising at least one of a sensing area and an emission area of each semiconductor device of the adjacent semiconductor devices.

26. (Previously presented) The method of claim 25, further comprising:
forming a redistribution layer over the active surface, at least one conductive trace of the redistribution layer extending at least partially over at least one semiconductor device of the adjacent semiconductor devices.

27. (Previously presented) The method of claim 25, further comprising:
removing the temporary protective layer.

28. (Previously presented) The method of claim 27, further comprising:
positioning an optically transparent lid over the optical element of at least one semiconductor device of the adjacent semiconductor devices.

29. (Previously presented) The method of claim 28, wherein positioning the optically transparent lid comprises positioning an optically transparent lid over optical elements of a plurality of the adjacent semiconductor devices.

30. (Previously presented) The method of claim 29, further comprising:
severing the optically transparent lid to form an individual optically transparent lid over each of the optical elements.

31. (Previously presented) The method of claim 30, wherein severing the optically transparent lid is effected substantially concurrently with exposing at least portions of at least some conductive elements.

32. (Previously presented) The method of claim 30, wherein severing the optically transparent lid comprises forming the individual optically transparent lid to include a peripheral edge that comprises at least one of a bevel and a chamfer.

33. (Previously presented) The method of claim 30, wherein forming the dielectric coating comprises severing dielectric material within at least one recess between the adjacent semiconductor devices after severing the optically transparent lid.

34. (Previously presented) The method of claim 28, wherein positioning the optically transparent lid comprises positioning an individual optically transparent lid over at least the optical element of the at least one semiconductor device, the individual optically transparent lid not extending over another semiconductor device of the adjacent semiconductor devices.

35. (Previously presented) The method of claim 28, further comprising:
forming a sacrificial layer over the optically transparent lid.

36. (Previously presented) The method of claim 35, wherein forming the peripheral section of the contact pad comprises:
forming a layer comprising conductive material over the sacrificial layer and on the peripheral edge;
patterning the layer comprising conductive material to form the peripheral section; and
removing the sacrificial layer and portions of the layer comprising conductive material that remain thereon.

37. (Previously presented) The method of claim 36, wherein removing comprises lifting the portions off of the optically transparent lid.

38-68 (Canceled)

69. (Previously presented) A method for fabricating a chip-scale package, comprising:
forming a redistribution layer on the active surface of a device substrate and in electrical isolation from circuitry of at least one underlying semiconductor device;

positioning a sacrificial substrate adjacent to a back side of the device substrate with a plurality of conductive elements on an active surface of the sacrificial substrate being aligned along at least one street between adjacent semiconductor devices on an active surface of the device substrate;

securing the active surface of the sacrificial substrate to the back side of the device substrate with a quantity of dielectric material electrically isolating each conductive element of the plurality of conductive elements from the back side of the device substrate;

severing the device substrate to physically separate the adjacent semiconductor devices from one another and to form peripheral edges of each semiconductor device of the adjacent semiconductor devices, relative positions of the adjacent semiconductor devices being maintained by the sacrificial substrate;

forming a dielectric coating on at least portions of at least some of the peripheral edges;

exposing at least portions of at least some conductive elements of the plurality of conductive elements, each exposed conductive element comprising a lower section of a contact pad of the chip-scale package; and

forming a peripheral section of the contact pad in communication with a corresponding lower section and on a peripheral edge of a semiconductor device.

70. (Previously presented) The method of claim 69, wherein forming the dielectric coating includes forming a dielectric coating over at least portions of the active surface of the device substrate.

71. (Previously presented) The method of claim 70, wherein forming the dielectric coating over at least portions of the active surface of the device substrate electrically isolates at least one conductive trace of the redistribution layer from circuitry of an underlying semiconductor device.

72. (Previously presented) The method of claim 69, wherein forming the redistribution layer is effected before severing.

73. (Previously presented) The method of claim 72, wherein severing includes severing at least one conductive trace of the redistribution layer.

74. (Previously presented) The method of claim 69, further comprising:
forming an upper section of the contact pad in communication with both the peripheral section and a conductive trace of the redistribution layer and over at least one semiconductor device of the adjacent semiconductor devices.

75. (Previously presented) The method of claim 69, further comprising:
forming an upper section of the contact pad in communication with the peripheral section and over at least one semiconductor device of the adjacent semiconductor devices.

76. (Previously presented) The method of claim 69, further comprising:
removing at least a portion of the sacrificial substrate to facilitate separation of the adjacent semiconductor devices from one another.

77. (Previously presented) The method of claim 76, wherein removing comprises substantially removing the sacrificial substrate.

78. (Previously presented) The method of claim 77, wherein substantially removing comprises back grinding the sacrificial substrate.

79. (Previously presented) The method of claim 69, wherein securing comprises use of a dielectric adhesive material.

80. (Previously presented) The method of claim 69, wherein severing is effected into the dielectric material.

81. (Previously presented) The method of claim 69, wherein forming the dielectric coating comprises introducing dielectric material into at least one recess formed during severing.

82. (Previously presented) The method of claim 81, wherein introducing comprises forming a layer comprising the dielectric material over at least a portion of the active surface of the device substrate.

83. (Previously presented) The method of claim 81, wherein introducing comprises introducing a dielectric polymer into the at least one recess.

84. (Previously presented) The method of claim 81, wherein introducing comprises substantially filling the at least one recess with the dielectric material.

85. (Previously presented) The method of claim 84, further comprising:
severing the dielectric material to re-separate the adjacent semiconductor devices from one another.

86. (Previously presented) The method of claim 85, wherein exposing is effected substantially concurrently with severing the dielectric material.

87. (Previously presented) The method of claim 69, wherein positioning comprises positioning the device substrate such that the at least one street is aligned over at least some conductive elements of the plurality of conductive elements.

88. (Previously presented) The method of claim 87, wherein exposing comprises severing the at least some conductive elements.

89. (Previously presented) The method of claim 69, wherein positioning comprises positioning the device substrate such that the at least one street is aligned between an adjacent pair of conductive elements of the plurality of conductive elements.

90. (Previously presented) The method of claim 69, further comprising:
forming a temporary protective layer over at least a portion of each of the adjacent semiconductor devices prior to forming the dielectric coating.

91. (Previously presented) The method of claim 90, wherein forming the temporary protective layer is effected prior to severing.

92. (Previously presented) The method of claim 91, wherein forming the temporary protective layer comprises forming the temporary protective layer over an optical element comprising at least one of a sensing area and an emission area of each semiconductor device of the adjacent semiconductor devices.

93. (Previously presented) The method of claim 92, further comprising:
removing the temporary protective layer.

94. (Previously presented) The method of claim 93, further comprising:
positioning an optically transparent lid over the optical element of at least one semiconductor device of the adjacent semiconductor devices.

95. (Previously presented) The method of claim 94, wherein positioning the optically transparent lid comprises positioning an optically transparent lid over optical elements of a plurality of the adjacent semiconductor devices.

96. (Previously presented) The method of claim 95, further comprising:
severing the optically transparent lid to form an individual optically transparent lid over each of the optical elements.

97. (Previously presented) The method of claim 96, wherein severing the optically transparent lid is effected substantially concurrently with exposing at least portions of at least some conductive elements.

98. (Previously presented) The method of claim 96, wherein severing the optically transparent lid comprises forming the individual optically transparent lid to include a peripheral edge that comprises at least one of a bevel and a chamfer.

99. (Previously presented) The method of claim 96, wherein forming the dielectric coating comprises severing dielectric material within at least one recess between the adjacent semiconductor devices after severing the optically transparent lid.

100. (Previously presented) The method of claim 94, wherein positioning the optically transparent lid comprises positioning an individual optically transparent lid over at least the optical element of the at least one semiconductor device, the individual optically transparent lid not extending over another semiconductor device of the adjacent semiconductor devices.

101. (Previously presented) The method of claim 94, further comprising:
forming a sacrificial layer over the optically transparent lid.

102. (Previously presented) The method of claim 101, wherein forming the peripheral section of the contact pad comprises:
forming a layer comprising conductive material over the sacrificial layer and on the peripheral edge;
patterning the layer comprising conductive material to form the peripheral section; and

removing the sacrificial layer and portions of the layer comprising conductive material that remain thereon.

103. (Previously presented) The method of claim 102, wherein removing comprises lifting the portions off of the optically transparent lid.